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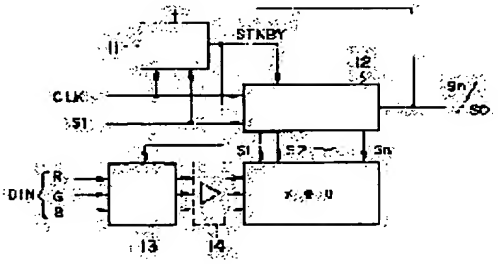
## (54) LIQUID CRYSTAL DISPLAY DEVICE AND ITS CONTROL METHOD

(57)Abstract:

PURPOSE: To drive it with low power even when a data frequency is accelerated by stopping the fetch of a liquid crystal display signal in a power down effective period without depending on only the stoppage of a clock signal related to power reduction in a liquid crystal display device.

CONSTITUTION: This device is provided with a signal generation circuit 11 identifying a fetching period of the liquid crystal display signal DIN and generating a stand-by signal STANBY, a shift register 12 generating internal clock signals S1-Sn from a reference signal CLK based on a start pulse S1 and the stand-by signal STANBY and a signal interruption circuit 13 stopping the fetch of the liquid crystal display signal DIN based on the stand-by signal STANBY, and the signal interruption circuit 13 is provided on the prestage of an input buffer circuit 14 receiving the liquid crystal display signal DIN.

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CLAIMS

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[Claim(s)]
[Claim 1] It is the liquid crystal display which is equipped with the signal generating circuit which identifies the incorporation period of a liquid crystal display signal, and generates a standby signal, the shift register which generates an internal clock signal from a reference signal based on a start pulse and said standby signal, and the signal cutoff circuit which stops the incorporation of a liquid crystal display signal based on said standby signal, and is characterized by to establish said signal cutoff circuit in the preceding paragraph of the input-buffer circuit which receives a liquid crystal display signal.
[Claim 2] The liquid crystal display according to claim 1 characterized by preparing the signal inverter circuit which reverses the signal logic of said liquid crystal display signal between said signal cutoff circuits and input-buffer circuits.
[Claim 3] It is the liquid crystal display which is equipped with the signal generating circuit which identifies the incorporation period of a liquid crystal display signal, and generates a standby signal, the shift register which generates an internal clock signal from a reference signal based on a start pulse and said standby signal, and the signal-control circuit which carries out the output control of said internal clock signal based on an enable signal and said standby signal, and is characterized by establishing said signal-control circuit in the preceding paragraph of the input-buffer circuit which receives an enable signal.
[Claim 4] The signal generating circuit which identifies the incorporation period of a liquid crystal display signal, and generates a standby signal, The shift register which generates an internal clock signal from a reference signal based on a start pulse and said standby signal, The signal cutoff circuit which stops the incorporation of a liquid crystal display signal based on said standby signal, It has the signal inverter circuit which reverses the signal logic of said liquid crystal display signal, and the signal-control circuit which carries out the output control of said internal clock signal based on an enable signal and said standby signal. It is the liquid crystal display characterized by establishing said signal inverter circuit in the preceding paragraph of the input-buffer circuit which receives a liquid crystal display signal, establishing said signal cutoff circuit in the preceding paragraph of a signal inverter circuit, and establishing said signal-control circuit in the preceding paragraph of the input-buffer circuit which receives an enable signal, respectively.
[Claim 5] Said signal generating circuits are one which is indicated to claims 1-4 characterized by identifying the period of the input point in time of the start pulse of said shift register to the output time of the start pulse of the shift register of the next step of liquid crystal displays.
[Claim 6] The control approach of the liquid crystal display characterized by identifying the incorporation period of a liquid crystal display signal, generating a standby signal, and stopping the incorporation of the liquid crystal display signal of a power down shelf-life based on said standby signal.
[Claim 7] The control approach of the liquid crystal display according to claim 6 characterized by stopping the parallel of a power down shelf-life, or the incorporation of a serial liquid crystal display signal based on said standby signal.

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[Translation done.]

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to low-power-ization of the display using a capacitative element as a storage means of image information, if it says in more detail about a liquid crystal display and its control approach. In recent years, the liquid crystal display (LCD:Liquid Crystal Display) of the active-matrix mold which integrated TFT (Thin Film Transistor) is manufactured with the high accumulation of semiconductor integrated circuit (it is called Following LSI) equipment, and development of a high density technique. LCD is spreading through the display of not only TV for home use but OA equipment from the display quality which is a thin light weight compared with CRT (cathode-ray tube), and is not inferior to CRT being acquired.
[0002] According to this, taking advantage of the point of a thin light weight, spreading widely as a display of a notebook computer is expected. In carrying out a dc-battery drive taking advantage of this portability, it becomes a technical problem how power consumption is stopped and a long duration continuation drive is enabled. Then, without being dependent only on a halt of a clock signal, the incorporation of the liquid crystal display signal of a power down shelf-life is stopped, and even if it is the case where the frequency of the data concerned is made into a high speed, the equipment and the approach of attaining low-power-ization are desired.
[0003]
[Description of the Prior Art] Drawing 15 -17 are an explanatory view concerning the conventional example. Drawing 15 (A) is the block diagram of the liquid crystal display unit concerning the conventional example, and drawing 15 (B) is the block diagram of the shift register of the data driver. Drawing 16 is the block diagram of a data driver, and drawing 17 shows the wave form chart of operation, respectively.
[0004] For example, the liquid crystal display unit which carries out a liquid crystal display based on a stairway electrical potential difference is equipped with the TFT substrate 1, the common electrode 2, the data driver 3, and scanning driver 4 grade as shown in drawing 15 (A). In the display panel which has the pixel electrode of 640 line x 480-pixel x3 color, the data driver 3 is put in order and formed at a time in the five vertical sections of the TFT substrate 1, and the one driver unit 3A has shift-register-circuit 3B, digital memory 3D, 3E, and decoding & selection circuit 3F, as shown in drawing 16.
[0005] Moreover, shift-register-circuit 3B is n flip-flops FF1-FFn (only henceforth FF circuit), and the clock control section 301, as shown in drawing 15 (B). It has. Next, the function of the data driver 3 of a liquid crystal display unit is explained. for example, a start pulse SI indicates it in shift-register-circuit 3B of each driver unit 3A as supply **** at drawing 17 (A) -- as -- a clock signal (henceforth a CLK signal) -- the control section 301 it asserts (effective) -- having -- a CLK signal -- synchronizing -- digital memory 3D from shift-register-circuit 3B -- control pulse signal S 1, S2, and ... Sn is outputted.
[0006] on the other hand, the liquid crystal display signal DIN from the outside (digital video signal = RDATA, GDATA, BDATA) carries out logic reversal synchronizing with the reversal control signal INV as shown in drawing 17 (B) by signal inverter circuit 3C -- having -- signal S 1 from after that and shift-register-circuit 3B, S2, and ... based on Sn, Data DIN are incorporated for it by 1st digital memory 3D of

driver unit 3A one by one.
[0007] Moreover, the CLK signal supplied to shift-register-circuit 3B while Signal Sn will be outputted as a start pulse SO of driver unit 3A of the next step, if the overflow signal Sn is outputted from FF circuit of the last stage of shift-register-circuit 3B is the control section 301. It is negated (invalid). Similarly, sequential negation of the 2nd - the 10th CLK signal of each driver unit 3A is carried out.
[0008] In addition, if the data DIN required for 1 level period memorized by digital memory 3D of each driver unit 3A are assembled, they will be transmitted to digital memory 3E of each driver unit 3A all at once, and each image data R, G, and B will be transmitted to decoding & selection circuit 3F based on the latch control signal LP. In circuit 3F, the reference voltages V1-Vm of m pieces are sampled, and the gradation electrical potential difference based on this is written in each pixel electrode through TFT of the bus line chosen by the scanning driver 4.
[0009] The charge by this is held at the distributed capacity of the pixel electrode until TFT of the following bus line is chosen. Information is maintained by this, the amount of transparency of light is controlled by what the inclination of the liquid crystal corresponding to this is decided for, and a gradation display is performed. In addition, the alternating current-ized drive which inverts the common electrical potential difference VCOM for degradation prevention of the liquid crystal itself and flicker prevention is taken.
[0010]
[Problem(s) to be Solved by the Invention] By the way, it has shift-register-circuit 3B as shown in each driver unit 3A at drawing 15 (B) according to the conventional example, and is the clock control section 301 there. It is prepared. moreover, as shown in drawing 17 (A), from the time of the input of a start pulse SI, signal Sn/SO is outputted and until, and a CLK signal confirm -- having -- other than this -- being alike -- supply of the CLK signal to the circuit 3B concerned is suspended.
[0011] This is for stopping the power consumption in the data driver 3, and only the period which is performing the ** 5 lump of Data DIN will operate shift-register-circuit 3B. Implementation of a low power-source drive is easy for this approach, and it is looked at by the digital driver built in pocket mold OA equipment. However, each driver unit 3A of every has the following problems only by the approach of stopping a CLK signal.
[0012] ** the period of negation of a CLK signal -- signal S 1 from shift-register-circuit 3B to digital memory 3D, S2, and ... although Sn has stopped, signal inverter circuit 3C prepared in the preceding paragraph of the memory 3D concerned and input-buffer circuit 3G are in operating state as before. The useless power consumption by this arises.
** When it is going to make highly minute the liquid crystal display panel used for pocket mold OA equipment etc. with increase of amount of information again, it is necessary to make high the handling frequency of the liquid crystal display signal DIN. For example, shortening of a level period is attained.
[0013] However, since the polarity reversals of the data DIN will be carried out, for example in signal inverter circuit 3C though it is the negation period of a CLK signal if a frequency is made high, the power consumed by the inverter circuit 3C concerned increases. This serves as a very big value, so that the handling frequency of Data DIN becomes a high speed. Moreover, the consumed electric current of input-buffer circuit 3G cannot be disregarded, either.
[0014] This becomes the hindrance of low-power-izing of pocket mold OA equipment, and it is not desirable in respect of the use continuity of the long duration which is the proposition of battery powered equipment. Without being created in view of the trouble of this conventional example, and being dependent only on a halt of a clock signal, this invention stops the incorporation of the liquid crystal display signal of a power down shelf-life, and even if it is the case where the frequency of the data concerned is made into a high speed, it aims at offer of the liquid crystal display which becomes possible [ attaining low-power-ization ], and its control approach.
[0015]
[Means for Solving the Problem] Drawing 1 and drawing 2 show the principle Fig. (1 the 2) of the liquid

crystal display concerning this invention, respectively. The signal generating circuit 11 which the 1st liquid crystal display of this invention identifies the incorporation period of the liquid crystal display signal DIN as shown in drawing 1 (A), and generates the standby signal STNBY, The shift register 12 which generates the internal clock signals S1-Sn from a reference signal CLK based on a start pulse S1 and said standby signal STNBY, It has the signal cutoff circuit 13 which stops the incorporation of the liquid crystal display signal DIN based on said standby signal STNBY, and said signal cutoff circuit 13 is characterized by being prepared in the preceding paragraph of the input-buffer circuit 14 which receives the liquid crystal display signal DIN.

[0016] The 2nd liquid crystal display of this invention is characterized by forming the signal inverter circuit 15 which reverses the signal logic of said liquid crystal display signal DIN between said signal cutoff circuits 13 and input-buffer circuits 14, as shown in drawing 1 (B). The signal generating circuit 11 which the 3rd liquid crystal display of this invention identifies the incorporation period of the liquid crystal display signal DIN as shown in drawing 2 (A), and generates the standby signal STNBY, The shift register 12 which generates the internal clock signals S1-Sn from a reference signal CLK based on a start pulse S1 and said standby signal STNBY, It has the signal-control circuit 16 which carries out the output control of said internal clock signals S1-Sn based on enable signals 1-EN 3 and said standby signal STNBY. Said signal-control circuit 16 It is characterized by being prepared in the preceding paragraph of the input-buffer circuit 17 which receives enable signals 1-EN 3.

[0017] The signal generating circuit 11 which the 4th liquid crystal display of this invention identifies the incorporation period of the liquid crystal display signal DIN as shown in drawing 2 (B), and generates the standby signal STNBY, The shift register 12 which generates the internal clock signals S1-Sn from a reference signal CLK based on a start pulse S1 and said standby signal STNBY, The signal cutoff circuit 13 which stops the incorporation of the liquid crystal display signal DIN based on said standby signal STNBY, The signal inverter circuit 15 which reverses the signal logic of said liquid crystal display signal DIN, It has the signal-control circuit 16 which carries out the output control of said internal clock signals S1-Sn based on enable signals 1-EN 3 and said standby signal STNBY. Said signal inverter circuit 15 is established in the preceding paragraph of the input-buffer circuit 14 which receives the liquid crystal display signal DIN. It is characterized by establishing said signal cutoff circuit 13 in the preceding paragraph of the signal inverter circuit 15, and establishing said signal-control circuit 16 in the preceding paragraph of the input-buffer circuit 17 which receives enable signals 1-EN 3, respectively.

[0018] In the 1st of this invention - the 4th liquid crystal display, said signal generating circuit 11 is characterized by identifying the period of the input point in time of the start pulse SI of said shift register 12 to the output time of start pulse Sn/SO of the shift register of the next step. The control approach of the liquid crystal display of this invention identifies the incorporation period of the liquid crystal display signal DIN, generates the standby signal STNBY, and is characterized by stopping the incorporation of the liquid crystal display signal DIN of a power down shelf-life based on said standby signal STNBY.

[0019] In the control approach of the liquid crystal display of this invention, it is characterized by stopping the parallel of a power down shelf-life, or the incorporation of the serial liquid crystal display signal DIN based on said standby signal STNBY, and the above-mentioned purpose is attained.

[0020]

[work --] for Actuation of the 1st liquid crystal display of this invention is explained. For example, in drawing 1 (A), if a start pulse SI is supplied to a signal generating circuit 11 and a shift register 12, the circuit 11 concerned will generate standby signal STNBY= "H" level, and will output it to a shift register 12 and the signal cutoff circuit 13, respectively.

[0021] Thereby, in the signal cutoff circuit 13 established in the preceding paragraph of the input-buffer circuit 14, incorporation of the liquid crystal display signal DIN of parallel is started based on STNBY= "H" level. If a shift register 12 is started based on a start pulse SI and STNBY= "H" level, the sequential shift of the reference signal CLK will be carried out with the register 12 concerned, for

example, specifically, n internal clock signals S1-Sn will be generated.
[0022] Based on these internal clock signals S1-Sn, the liquid crystal display signal DIN of parallel is stored in memory one by one. Moreover, if clock signal Sn/SO is outputted to the shift register of the next step from the last stage of a register 12, a signal generating circuit 11 will generate standby signal STNBY= "L" level, and will output it to the signal cutoff circuit 13. In the cutoff circuit 13 concerned, in order to enter at a power down shelf-life, incorporation of the liquid crystal display signal DIN is suspended. In addition, a power down shelf-life means a STNBY="L" level period, and, as for the period concerned, power down becomes an invalid with STNBY= "H" level.
[0023] For this reason, in a STNBY="L" level period, while the internal clock signals S1-Sn of a register 12 are stopped, the incorporation of the liquid crystal display signal DIN itself is suspended. The input-buffer circuit 14 established in the latter part of the signal cutoff circuit 13 can be made into non-operating state by this, and even if it is the case of the high-speed liquid crystal display signal DIN where it is dealt with, it becomes possible to reduce the consumed electric current of the circuit 14 concerned.
[0024] According to the 2nd liquid crystal display of this invention, as shown in drawing 1 R> 1 (B), the signal inverter circuit 15 which reverses the signal logic of the liquid crystal display signal DIN is formed between the signal cutoff circuit 13 and the input-buffer circuit 14. For this reason, in a STNBY="L" level period, while the internal clock signals S1-Sn are stopped like the 1st equipment, the conventional example enables it to suspend the incorporation of the liquid crystal display signal DIN by which polarity reversals were carried out [ be / it / under / 1 level period / letting it pass ] in the signal inverter circuit 15 itself.
[0025] The input-buffer circuit 14 and the signal inverter circuit 15 which were established in the latter part of the signal cutoff circuit 13 can be made into non-operating state by this, for example, the consumed electric current is contributed to reduction-ization compared with the liquid crystal display of the transparency mold of the conventional example. Actuation of the 3rd liquid crystal display of this invention is explained. For example, in drawing 2 (A), if a start pulse SI is supplied to a signal generating circuit 11 and a shift register 12, the circuit 11 concerned will generate standby signal STNBY= "H" level, and will output it to a shift register 12 and the signal-control circuit 16, respectively.
[0026] Thereby, in the signal-control circuit 16 established in the preceding paragraph of the input-buffer circuit 17, incorporation of the liquid crystal display signal DIN is started based on STNBY= "H" level. If a shift register 12 is started based on a start pulse SI and STNBY= "H" level, the sequential shift of the reference signal CLK will be carried out with the register 12 concerned, for example, specifically, n internal clock signals S1-Sn will be generated.
[0027] Based on enable signals EN1-EN3, as for these internal clock signals S1-Sn, the serial liquid crystal display signal DIN is stored in memory. Moreover, if clock signal Sn/SO is outputted to the shift register of the next step from the last stage of a register 12, a signal generating circuit 11 will generate standby signal STNBY= "L" level, and will output it to the signal-control circuit 16. In the control circuit 16 concerned, incorporation of the serial liquid crystal display signal DIN of a power down shelf-life is suspended.
[0028] For this reason, in a STNBY="L" level period, while the internal clock signals S1-Sn are stopped like the 1st and 2nd equipment, it becomes possible to incorporate for every R of the liquid crystal display signal DIN, G, and B data, and to stop the very thing. The input-buffer circuit 17 established in the latter part of the signal-control circuit 16 can be made into non-operating state by this, for example, it contributes to reduction-ization of the consumed electric current compared with the liquid crystal display of the projection mold of the conventional example.
[0029] According to the 4th liquid crystal display of this invention, as shown in drawing 2 R> 2 (B), the signal cutoff circuit 13 is established in the preceding paragraph of the signal inverter circuit 15, and the signal-control circuit 16 is established in the preceding paragraph of the input-buffer circuit 17, respectively. For this reason, in a STNBY="L" level period, while the internal clock signals S1-Sn are

stopped like the 2nd and 3rd equipment, it becomes possible to incorporate for every R of the liquid crystal display signal DIN, G, and B data, and to stop the very thing.
[0030] To make into non-operating state by this the input-buffer circuit 14 established in the latter part of the signal cutoff circuit 13 and the signal inverter circuit 15 and the input-buffer circuit 17 established in the latter part of the signal-control circuit 16 can be made into non-operating state, respectively, and the consumed electric current in the liquid crystal display concerned is contributed to reduction-ization compared with the conventional example. Auto power down more effective than the conventional example can be realized without being dependent on actuation from the exterior by equipping the liquid crystal display concerned with the control approach which carries out an incorporation halt of the liquid crystal display signal DIN to such a power down shelf-life.
[0031]
[Example] Next, each example of this invention is explained, referring to drawing. Drawing 3 -14 are drawing explaining the liquid crystal display concerning the example of this invention, and its control approach.
(1) The explanatory view 3 of the 1st example is the whole liquid crystal display unit block diagram concerning each example of this invention, and drawing 4 is the electrode explanatory view of the liquid crystal display panel. Drawing 5 is the block diagram of the data driver concerning the 1st example, and drawing 6 (A) and (B) are the power down circuit and the internal configuration Fig. of a shift register. Drawing 7 (A) is the internal configuration Fig. of the video-signal cutoff circuit concerning the 1st example of this invention, and drawing 8 shows the wave form chart of the data driver concerning the 1st example of operation, respectively.
[0032] For example, based on eight kinds of reference voltages V0-V7, the liquid crystal display unit which holds any one stairway electrical potential difference in a stair-like wave electrical potential difference to distributed capacity is equipped with the TFT substrate 31, the common electrode 32, the data driver 33, and scanning driver 34 grade, as shown in drawing 3 . It has the scanning bus line (scan electrode) SBL and the data bus line (signal electrode) DBL which were prepared in the shape of a matrix, a switching element (TFT) is connected at the intersection of these Rhine, and the TFT substrate 31 changes, as shown in drawing 4 . A pixel electrode is connected to the TFT concerned.
[0033] The common electrode 32 is formed in the TFT substrate 31 at a lower layer, and liquid crystal is enclosed between this substrate 31 and electrode 32. The common electrical potential difference VCOM is supplied to an electrode 32. The scanning driver 34 chooses TFT connected to the scanning bus line SBL in response to scanning clock signal CLKS and scanning pulse signal SPS. Moreover, in the display panel which has the pixel electrode of 640 line x 480-pixel x3 color, the data driver 33 is divided and formed at a time in the five vertical sections of the TFT substrate 31, and the one driver unit 33 has the power down circuit 21, a shift register circuit 22, the video-signal cutoff circuit 23, the digital memory 28 and 29, and the decoding & selection circuit 30, as shown in drawing 5 .
[0034] The power down circuit 21 is an example of the signal generating circuit 11 of drawing 1 (A), identifies the incorporation period of the liquid crystal display data RDATA, GDATA, and BDATA of 3 dots (only henceforth DIN), and generates a standby signal (only henceforth a STNBY signal). for example, the circuit 21 concerned is shown in drawing 6 (A) -- as -- flip-flop circuit 201 And reset set circuit 202 from -- it changes.
[0035] Circuit 201 A reset signal is generated based on a reference clock signal (only henceforth a CLK signal), and start signal SO of the next step, and it is a circuit 202 about it. It outputs. Circuit 202 A STNBY signal is generated based on a reset signal and start signal SI. In a shift register circuit 22, the period of the output time of start pulse Sn/SO from the input point in time of a start pulse SI to the shift register of a next step driver is identified.
[0036] By this, the incorporation period of the liquid crystal display data DIN of parallel can be identified, a STNBY signal can be generated, and the incorporation of the liquid crystal display data DIN of a power down shelf-life can be stopped based on a STNBY signal. A shift register circuit 22 is an example of the

shift register 12 of drawing 1 (A), and generates the internal clock signals S1-Sn from a CLK signal based on a start pulse SI (SP) and a STNBY signal. For example, a shift register circuit 22 is a gate circuit 203, as shown in drawing 6 (B). And it consists of n flip-flop circuits FF1-FFn (only henceforth FF circuit). Circuit 203 The output control of a CLK signal is carried out based on a STNBY signal.

[0037] The video-signal cutoff circuit 23 is an example of the signal cutoff circuit 13, and is a data control circuit which stops the incorporation of the liquid crystal display data DIN based on a STNBY signal. for example, the video-signal cutoff circuit 23 is shown in drawing 7 (A) -- as -- three 2 input NAND circuits 204-206 And inverter 207-209 from -- it changes. NAND circuit 204 Based on a STNBY signal, passage control of RDATA (red image data) is carried out, and it is an inverter. 207 reverses the signal logic. NAND circuit 205 carries out passage control of GDATA (green image data) based on a STNBY signal, and is an inverter. 208 reverses the signal logic. Similarly, it is NAND circuit 206. Based on a STNBY signal, passage control of BDATA (blue image data) is carried out, and it is an inverter. 209 reverses the signal logic.

[0038] The signal cutoff circuit 23 concerned is established in the preceding paragraph of the input-buffer circuit 24 which receives the liquid crystal display data DIN. A buffer circuit 24 amplifies Data DIN and transmits it to the digital memory 28. The digital memory 28 stores RDATA, GDATA, and BDATA temporarily based on the internal clock signals S1-Sn. R, G, and BDATA are digital video signals. the digital memory 29 -- the liquid crystal display data R1 and G1 of the pixel [ 1st ] triplet from memory 28, and B1- when the pixel [ n-th ] liquid crystal display data Rn, Gn, and Bn are stored temporarily and the liquid crystal display data of 1 level period are assembled, based on the latch control signal LP, these 3xn data R1-Rn, G1-Gn, and B1-Rn are transmitted to the decoding & selection circuit 30.

[0039] The decoding & selection circuit 30 decodes 3xn data R1-Rn, G1-Gn, and B1-Rn, chooses reference voltages V0-V7, generates a stair-like wave electrical potential difference, and writes in TFT by which it was connected to the data bus line DBL. Moreover, this information is suppressed by the driver 33 in the amplitude range of a gradation electrical potential difference less than [ 5V ]. The drive power source VCC of a driver 33 is single -5V.

[0040] Next, the actuation at the time of the low power drive of the liquid crystal display concerning the 1st example of this invention is explained. For example, if the start pulse SI as shown in the power down circuit 21 and a shift register circuit 22 at drawing 8 is supplied synchronizing with falling of Horizontal Synchronizing signal HSYNC, the circuit 21 concerned will generate STNBY signal = "H" level, and will output it to a shift register circuit 22 and the video-signal cutoff circuit 23, respectively.

[0041] This is based on STNBY= "H" level in the video-signal cutoff circuit 23 established in the preceding paragraph of the input-buffer circuit 24, and it is liquid crystal display data DIN=R1 of parallel, and G1 and B1. -- Incorporation is started. If a shift register circuit 22 is started based on a start pulse SI and STNBY= "H" level, the sequential shift of the CLK signal will be carried out by the register circuit 22 concerned, for example, a CLK signal will be incorporated only for the period of STNBY= "H" level in a register circuit 22, and, specifically, n internal clock signals S1-Sn will be generated only for the period.

[0042] Based on these internal clock signals S1-Sn, the liquid crystal display data DIN (RM, GM, BM) are stored in memory 28. Moreover, if clock signal Sn/SO is outputted to the shift register of the next step from the last stage of a register circuit 22, the power down circuit 21 will generate STNBY signal = "L" level, and will output it to the video-signal cutoff circuit 23.

[0043] In the cutoff circuit 23 concerned, incorporation of the liquid crystal display data DIN of a power down shelf-life is suspended. That is, it enters with STNBY= "L" level at a power down shelf-life, and it becomes an invalid with STNBY= "H" level. Thereby, a high-speed video signal can be abolished for signal change in the preceding paragraph of the input-buffer circuit 24. In addition, the contents of the digital memory 28 are transmitted to the digital memory 29 by the latch control signal LP, and the reference voltages V0-V7 corresponding to the contents are chosen.

[0044] Thus, according to the liquid crystal display concerning the 1st example of this invention, as

shown in drawing 5 , it has the power down circuit 21, a shift register circuit 22, and the video-signal cutoff circuit 23, and the cutoff circuit 23 concerned is established in the preceding paragraph of the input-buffer circuit 24 which receives the liquid crystal display data DIN. For this reason, a power down period becomes effective by last stage output Sn/SO of a shift register circuit 22, and the STNBY signal canceled by the start pulse SI is created by the power down circuit 21. By this, by the STNBY="L" level period, while the internal clock signals S1-Sn of a register circuit 22 are stopped, the incorporation of the liquid crystal display data DIN itself is suspended.

[0045] The input-buffer circuit 24 established in the latter part of the video-signal cutoff circuit 23 can be made into non-operating state by this, and even if it is the case of the high-speed liquid crystal display data DIN where it is dealt with, it becomes possible to reduce the consumed electric current of the circuit 24 concerned. Low-power-ization of pocket mold OA equipment is attained and the place which contributes to the point of the use continuity of the long duration which is the proposition of battery powered equipment is large at this.

[0046] Furthermore, 1 level period is shortened, high resolution-ization is attained by making the frequency of a video signal high, and it becomes possible to cope with enough highly-minute-izing of a liquid crystal display panel and pocket mold OA equipment accompanying increase of amount of information.

(2) The explanatory view 7 of the 2nd example (B) is an internal configuration Fig. of the video-signal inverter circuit concerning the 2nd example of this invention, and drawing 9 is the block diagram of the data driver concerning the 2nd example. Drawing 10 (A) is the wave form chart of operation, and drawing 10 (B) shows the relation of the level period and reversal control signal supplementary to the wave of operation, respectively.

[0047] In the example of different **** 2 from the 1st example, the data inverter circuit (INV) 25 which reverses the signal logic of the liquid crystal display data DIN is formed between the video-signal cutoff circuit 23 and the input-buffer circuit 24. That is, the data inverter circuit 25 consists of the 2 input EXOR (exclusive OR) circuits 51-53, as it is an example of the signal inverter circuit 15 of drawing 1 (B), for example, is shown in drawing 7 (B). The EXOR circuit 51 reverses RDATA based on a reversal control signal (henceforth an INV signal), the EXOR circuit 52 reverses GDATA based on an INV signal, and the EXOR circuit 53 reverses BDATA based on an INV signal, respectively. The data inverter circuit 25 concerned is established in the preceding paragraph of the input-buffer circuit 24 which receives the liquid crystal display data DIN. Since the thing of the other same notations and the same name is the same as that of the 1st example, the explanation is omitted.

[0048] Next, the actuation at the time of the low power drive of the liquid crystal display concerning the 2nd example of this invention is explained. For example, if the start pulse SI as shown in drawing 10 (A) is supplied to the power down circuit 21 and a shift register circuit 22 like the 1st example, the circuit 21 concerned will generate STNBY signal = "H" level, and will output it to a shift register circuit 22 and the video-signal cutoff circuit 23, respectively.

[0049] Thereby, in the video-signal cutoff circuit 23 established in the preceding paragraph of the data inverter circuit 25, incorporation of the liquid crystal display data DIN is started based on STNBY= "H" level. If a shift register circuit 22 is started based on a start pulse SI and STNBY= "H" level, n internal clock signals S1-Sn will be outputted to the digital memory 28 from the register circuit 22 concerned.

[0050] Based on these internal clock signals S1-Sn and an INV signal, the liquid crystal display data DIN by which polarity reversals were carried out for every 1 level period in the data inverter circuit 25 are stored in memory. Moreover, if clock signal Sn/SO is outputted to the shift register of the next step from the last stage of a register circuit 22, the power down circuit 21 will generate STNBY signal = "L" level, and will output it to the video-signal cutoff circuit 23. While the internal clock signals S1-Sn become an invalid on STNBY signal = "L" level, in the cutoff circuit 23 concerned, incorporation of the liquid crystal display data DIN of a power down shelf-life is suspended. Then, the contents of the digital memory 28 are transmitted to the digital memory 29 by the latch control signal LP, and the reference

voltages V0-V7 corresponding to the contents are chosen.
[0051] Thus, according to the liquid crystal display concerning the 2nd example of this invention, as shown in drawing 9 , the data inverter circuit 25 which reverses the signal logic of the liquid crystal display data DIN is formed between the video-signal cutoff circuit 23 and the input-buffer circuit 24. For this reason, when a STNBY signal is "H" level, the data inverter circuit 25 is made into operating state, logic reversal of the data DIN is carried out by INV signal = "H" level, and when it is "L" level, the data DIN of noninverting logic are stored in the digital memory 28. In a STNBY="L" level period, this enables it to suspend the incorporation of the liquid crystal display data DIN by which polarity reversals are carried out for every 1 level period in the signal inverter circuit 15 itself, while the internal clock signals S1-Sn are stopped like the 1st example.
[0052] The data inverter circuit 25 and the input-buffer circuit 24 which were established in the latter part of the video-signal cutoff circuit 23 can be made into non-operating state by this, and it becomes possible to reduce the consumed electric current of the circuits 24 and 25 concerned compared with the conventional example. The non-operating period of the inverter circuit 25 concerned acts effective in low consumerization, so that the handling frequency of Data DIN becomes a high speed. Compared with the liquid crystal display of the transparency mold of the conventional example, power consumption is contributed to reduction-ization.
[0053] (3) The explanatory view 11 of the 3rd example is a block diagram of the data driver concerning the 3rd example of this invention, and drawing 12 is the internal configuration Fig. of the enabling control circuit. Drawing 13 (A) is the wave form chart of operation, and drawing 13 (B) shows the relation of the level period and reversal control signal supplementary to the wave of operation, respectively.
[0054] In the example of different **** 3 from the 1st and 2nd example, the enabling control circuit 26 is formed in the preceding paragraph of input-buffer circuit 27A which receives enable signals (internal supply) EN1-EN3. That is, the enabling control circuit 26 is an example of the signal-control circuit 16 of drawing 2 (A), and carries out the output control of the internal clock signals S1-Sn based on enable signals EN1-EN3 and a STNBY signal. For example, a control circuit 26 consists of three 2 input NAND circuits 61-63 and inverters 64-66, as shown in drawing 12.
[0055] NAND circuit 61 carries out passage control of an enable signal EN1 based on a STNBY signal, and an inverter 64 reverses the signal logic. NAND circuit 62 carries out passage control of an enable signal EN2 based on a STNBY signal, and an inverter 65 reverses the signal logic. Similarly, NAND circuit 63 carries out passage control of an enable signal EN3 based on a STNBY signal, and an inverter 66 reverses the signal logic.
[0056] The circuit 26 concerned is established in the preceding paragraph of input-buffer circuit 27A which receives enable signals EN1-EN3, and buffer circuit 27A amplifies signals EN1-EN3, and transmits it to 3xn gate circuit 27B respectively. Gate circuit 27B carries out the output control of the internal clock signals S1-Sn from a shift register circuit 22 based on the signals EN1-EN3 which became effective. This is controlling the pulse width of the output signal of a shift register circuit 22, and is for switching the function to incorporate a triplet (RGB) to coincidence, and the function to incorporate data for every bit.
[0057] Since the thing of the other same notations and the same name is the same as that of the 1st and 2nd example, the explanation is omitted. Next, the actuation at the time of the low consumption drive of the liquid crystal display concerning the 3rd example of this invention is explained. For example, if the start pulse SI as shown in drawing 13 (A) is supplied to the power down circuit 21 and a shift register circuit 22 like the 1st and 2nd example, the circuit 21 concerned will generate STNBY signal = "H" level, and will output it to a shift register circuit 22 and the enabling control circuit 26, respectively.
[0058] Thereby, in a control circuit 26, incorporation of the liquid crystal display data DIN is started based on STNBY= "H" level. If a shift register circuit 22 is started based on a start pulse SI and STNBY= "H" level, the sequential shift of the CLK signal will be carried out by the register circuit 22 concerned, for example, specifically, n internal clock signals S1-Sn will be outputted to 3xn gate circuit

27B.
[0059] Serial RDATA will be incorporated by the digital memory 28, if it confirms with an enable signal EN1 in 1 level period as these internal clock signals S11-Sn1 are shown in drawing 13 (B). Moreover, serial GDATA will be incorporated by the digital memory 28 if signals S12-Sn2 are confirmed based on an enable signal EN2. Similarly, serial BDATA will be incorporated by the digital memory 28 if signals S13-Sn3 are confirmed based on an enable signal EN3. Moreover, if signals EN1-EN3 and a CLK signal are made into a same waveform, the data DIN of 3 dots will be crowded in the digital memory 28 coincidence picking like the 1st and 2nd examples.
[0060] In addition, if clock signal Sn/SO is outputted to the shift register of the next step from the last stage of a register circuit 22, the power down circuit 21 will generate STNBY signal = "L" level, and will output it to the enabling control circuit 26. Thereby, the CLK signal of a shift register circuit 22 and enable signals EN1-EN3 become an invalid. Incorporation of the serial liquid crystal display data DIN in a power down shelf-life is suspended. Then, the contents of the digital memory 28 are transmitted to the digital memory 29 by the latch control signal LP, and the reference voltages V0-V7 corresponding to the contents are chosen.
[0061] Thus, according to the liquid crystal display unit concerning the 3rd example of this invention, as shown in drawing 11, the enabling control circuit 26 is formed in the preceding paragraph of input-buffer circuit 27A which receives enable signals EN1-EN3. For this reason, in a STNBY="L" level period, while the internal clock signals S1-Sn of a register circuit 22 are stopped, signals EN1-EN3 become an invalid, the output of gate circuit 27B is suspended, and the incorporation of serial liquid crystal display data, such as RDATA, GDATA, or BDATA, itself is suspended. Input-buffer circuit 27A prepared in the latter part of a control circuit 26 can be made into non-operating state by this, and it becomes possible in a STNBY="L" level period to reduce the consumed electric current of the circuit 27A concerned like the 1st and 2nd examples. Compared with the liquid crystal display of the projection mold of the conventional example, power consumption is contributed to reduction-ization.
[0062] (4) The explanatory view 14 of the 4th example shows the block diagram of the data driver concerning the 4th example of this invention. In the 4th example, the 2nd and 3rd examples are put together. That is, the data inverter circuit 25 is established in the preceding paragraph of the input-buffer circuit 24 which receives the liquid crystal display data DIN, the video-signal cutoff circuit 23 is established in the preceding paragraph of the data inverter circuit 25, and the enabling control circuit 26 is formed in the preceding paragraph of input-buffer circuit 27B which receives enable signals EN1-EN3, respectively.
[0063] For this reason, in a STNBY="L" level period, like the 2nd and 3rd example, while the internal clock signals S1-Sn are stopped, it becomes possible to incorporate for every R of the liquid crystal display data DIN, G, and B data, and to stop the very thing. To make the input-buffer circuit 24 and the data inverter circuit 25 into non-operating state and input-buffer circuit 27A can be made into non-operating state by this, respectively, and it becomes possible to reduce the power consumption of a liquid crystal display unit compared with the conventional example.
[0064] Thus, in each example of this invention, the data driver 33 used for one panel has an automatic power down function respectively. [ two or more ] All the signals (a video signal, enable signal, etc.) supplied to the driver 33 interior are controllable by this with the STNBY signal from the power down circuit 21. Thereby, without being dependent on external actuation, the relay action of two or more data drivers 33 can be carried out to 1 level period, and reduction-ization of large power consumption can be attained rather than the conventional example.
[0065]
[Effect of the Invention] According to the liquid crystal display of this invention, it has a signal generating circuit, a shift register, and a signal cutoff circuit, and the cutoff circuit concerned is established in the preceding paragraph of the input-buffer circuit which receives a liquid crystal display signal. For this reason, while the internal clock signal of a register is stopped in a power down shelf-life

based on the standby signal from a signal generating circuit, the incorporation of a liquid crystal display signal itself is suspended by the signal cutoff circuit, and the input-buffer circuit of the latter part of a signal cutoff circuit can be made into non-operating state.

[0066] According to other liquid crystal displays of this invention, a signal cutoff circuit is established in the preceding paragraph of the signal inverter circuit which reverses the signal logic of a liquid crystal display signal. For this reason, in a power down shelf-life, while an internal clock signal is stopped, it is stopped by the signal cutoff circuit and the incorporation of a liquid crystal display signal by which polarity reversals are carried out for every 1 level period can make the signal inverter circuit of the latter part of a signal cutoff circuit non-operating state.

[0067] According to other liquid crystal displays of this invention, the signal-control circuit which carries out the output control of the enable signal based on a standby signal is established in the preceding paragraph of an input-buffer circuit. For this reason, in a power down shelf-life, while an internal clock signal is stopped, incorporation can be suspended for every serial data of a liquid crystal display signal, and the input-buffer circuit of the latter part of a signal-control circuit can be made into non-operating state.

[0068] According to the control approach of the liquid crystal display of this invention, the incorporation period of a liquid crystal display signal is identified, a standby signal is generated, and the parallel of a power down shelf-life or the incorporation of a serial liquid crystal display signal is stopped based on this signal. For this reason, even if it is the case of a high-speed liquid crystal display signal where it is dealt with, the consumed electric current of the equipment concerned can be held down to necessary minimum, and it becomes possible to reduce the consumed electric current in each circuit. And automatic power down with an easy configuration is realized.

[0069] This contributes to low power consumption-ization of the liquid crystal display of a transparency mold and a projection mold. Moreover, it contributes to offer of the pocket mold OA equipment in which long duration use is possible greatly.

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[Translation done.]



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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1] It is the principle Fig. (the 1) of the liquid crystal display concerning this invention.

[Drawing 2] It is the principle Fig. (the 2) of the liquid crystal display concerning this invention.

[Drawing 3] It is the whole liquid crystal display unit block diagram concerning each example of this invention.

[Drawing 4] It is the electrode explanatory view of the liquid crystal display panel concerning each example of this invention.

[Drawing 5] It is the block diagram of the data driver concerning the 1st example of this invention.

[Drawing 6] It is the internal configuration Fig. of the power down circuit concerning each example of this invention, and a shift register circuit.
[Drawing 7] It is the internal configuration Fig. of the video-signal cutoff circuit concerning the example of this invention, and a data inverter circuit.
[Drawing 8] It is the wave form chart of the data driver concerning the 1st example of this invention of operation.
[Drawing 9] It is the block diagram of the data driver concerning the 2nd example of this invention.
[Drawing 10] It is the wave form chart of the data driver concerning the 2nd example of this invention of operation.
[Drawing 11] It is the block diagram of the data driver concerning the 3rd example of this invention.
[Drawing 12] It is the internal configuration Fig. of the enabling control circuit concerning the 3rd example of this invention.
[Drawing 13] It is the wave form chart of the data driver concerning the 3rd example of this invention of operation.
[Drawing 14] It is the block diagram of the data driver concerning the 4th example of this invention.
[Drawing 15] It is the explanatory view of the liquid crystal display unit concerning the conventional example, and the power down approach.
[Drawing 16] It is the internal configuration Fig. of the data driver concerning the conventional example.
[Drawing 17] It is the wave form chart of the data driver concerning the conventional example of operation.
[Description of Notations]
11 -- Signal generating circuit,
12 -- Shift register,
13 -- Signal cutoff circuit,
14 17 -- Input-buffer circuit,
15 -- Signal inverter circuit,
16 -- Signal-control circuit,
STNBY -- Standby signal,
S1-Sn -- Internal clock signal,
EN1-EN3 -- Enable signal
SI (SP) -- Start pulse,
Sn/SO -- Start pulse of the next step,
INV -- Reversal control signal.

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[Translation done.]